REMARKS

Claim 35 has been amended. Claim 36 has been canceled. Claims 1-23, 35 and 37-40 are currently pending in this application.

Claim 19 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Smith, U.S. Patent No. 5,808,874 (Smith I). This rejection is respectfully traversed.

Independent claim 19 recites a "method of making semiconductor device packages, comprising: aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape; subsequently, connecting said semiconductor devices in said wafer to ball grid arrays on said dielectric tape; and simultaneously dicing said wafer and said dielectric tape."

Smith I fails to disclose all limitations of claim 19. Smith relates to mounting and connection devices and techniques for use with microelectronic elements such as semiconductor chips. Smith I at col. 1, lines 5-7. Smith I discloses that two elements are provided, each with interior confronting surfaces having contacts. Smith I vat col. 6, lines 20-46. The contacts have a fusible metal disposed thereon. Smith I at col. 7, lines 1-6. The contacts of each element are aligned with one another and a fusible conductive material is disposed therebetween. Smith I at col. 8, lines 24-39. In contrast, claim 19 recites "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape." Therefore, Smith I does not disclose all limitations of claim 19. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith I in view of Gaynes et al., U.S. Patent No. 6,165,885 (Gaynes). This rejection is respectfully traversed.

Claim 20 depends from claim 19. For at least the reasons discussed above, Smith I fails to disclose, teach or suggest all limitations of claim 19. Gaynes is cited for teaching optical alignment of connectors on an attachment substrate with interconnectors of a chip carrier substrate. Gaynes at col. 17, line 50 to col. 18, line 65. Thus, Gaynes does not supplement the deficiencies of Smith I. Therefore, even when considered in combination, Smith I and Gaynes fail to teach or suggest all limitations of claims 19 and 20.

Claims 21-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith I in view of Smith, U.S. Patent No. 6,300,149 (Smith II). This rejection is respectfully traversed.

Claims 21-23 depends from claim 19. For at least the reasons discussed above, Smith I fails to disclose, teach or suggest all limitations of claim 19. Smith II is cited for teaching lattice alignment of individual semiconductor device elements within a field. Smith II at col. 3, line 14 to col. 4, line 67. Thus, Smith II does not supplement the deficiencies of Smith I. Therefore, even when considered in combination, Smith I and Smith II fail to teach or suggest all limitations of claims 19 and 21-23.

Claims 1-18 and 35-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi et al., U.S. Patent No. 6,297,553 in view of Smith I. This rejection is respectfully traversed.

Independent claim 1 recites a "method of making semiconductor device packages comprising, *inter alia*, "testing semiconductor devices in said wafer" and "subsequently, dicing said layered assembly." Independent claim 11 recites a "method of making semiconductor device packages" comprising, *inter alia* "determining whether the wafer contains a defective semiconductor device" and "subsequently, dicing said

layered assembly." Similarly, as amended, independent claim 35 recites a "method of handling a plurality of semiconductor devices arrayed in a semiconductor wafer" comprising, *inter alia,* "testing said semiconductor devices through said ball grid arrays" and "subsequently, singulating packages from said wafer and said substrate.

As acknowledged by the examiner, Horiuchi does not teach or suggest testing semiconductor devices through input/output devices. Office Action at 7. Horiuchi is silent about testing semiconductor devices in any way. Smith I teaches testing semiconductor chips through terminals 17. Smith I, however, teaches that the testing is conducted of individual finished units 58, which have been severed from the wafer 22. Smith I at col. 11, lines 20-26; col. 13, lines 12-24. Thus, like Horiuchi, Smith I fails to teach or suggest testing semiconductor devices prior to a dicing or singulating process. Therefore, even when considered in combination, Horiuchi and Smith I fail to teach or suggest all limitations of any of independent claims 1, 11 and 35. For at least these reasons, withdrawal of this rejection is respectfully requested.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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